Performance Comparison of 7-level Multi-Level Inverter Topologies using FPGA

R.Nithya[a*], Research Scholar, Department of Electronics and Instrumentation Engineering, Annamalai University, Chidambaram, Tamil Nadu, India. email: nithiazure@gmail.com
Dr. T. Anitha[b], Associate Professor, Department of Electronics and Instrumentation Engineering, Annamalai University, Chidambaram, Tamil Nadu, India. email: rgm_anitha@rediffmail.com
Dr.M.Arulaalan[c],Professor, Department of Electronics and Communication Engineering, C K College of Engineering & Technology, Cuddalore, Tamil Nadu, India. email: arulaalan@gmail.com

Abstract:-This paper compares the Multi-Level Inverter namely Switched Ladder and H-Bridge Topologies for the performance parameters. The topologies considered are fed with the switch patterns from the non-carrier angle manipulated formula. The switching angle algorithm identifies on which particular angle the signal has to be generated. It is identified based on four algorithm namely half height method, equal phase method,This paper concentrates on the 7-level MLI AC output using the synthesizable VHDL code and implemented using the FPGA in real-time. For verification in simulation, the cross-compiling is attained using the System Generator tool.

Keywords: Switched Ladder Inverter Topology, H-Bridge Inverter Topology, Switching Angle Method, Field Programmable Gate Array

I. INTRODUCTION

The Multi-level Inverter is a power circuit used for converting the DC to AC output. The MLI requires switch patterns for generating the level of the AC output. Based on the switching and topology used, the MLI circuit can be categorized..The PWM signal is a signal suitable for the MLI to be converted to produce a PWM signal, which is a high carrier overlapping signal. The signal instructions of MLI are defined as phase configuration, phase configuration and variable phase-counter configuration. In recent years, carrier-free PWM generation has been used to control MLI circuits.

This non-carrier-based PWM is generated by the happening of ON and OFF periods on the digital scale for the sake of coding. A variable angle can be defined for each quadrant of the AC output depending on the number of degrees.The non-carrier switching angle algorithm is advantageous in comparison to the carrier-based method for the following reasons; i) accuracy in the generation of the triggering angles, ii) low%THD for any level of the inverter irrespective of the topology used, and iii) ease in designing using compatible digital controllers. The other aspect of the inverter classification is the topology of the circuitry.

The MLI classification based on topology depends on the type of circuitry and the number of switches used. The need for MLI topology design is to achieve lower cost and higher performance through optimization of components [1]. Although many inverters are classified by the number of devices used, their size and design are not straightforward; The MLI topology is designed to account for the reduced number of switches [2]. MLI topology with reduced switching and DC voltage is suitable for many switching applications [3]. Inverter topologies based on low voltage devices can use fewer switches and DC voltage and have very low stress [4]. Dual-source-based MLI uses low-power transformers to operate symmetrically and asymmetrically to suit rooftop PV applications [5]. A low THD% output ladder can be produced by using a suitable switching device [6].The switched ladder topology

has the adaptability to various voltage ratios and the placement of DC sources with fewer power switching components [7]. The reduction in switched ladder-based MLI achieves enhanced output level helping in a smooth transition and diminished%THD of the AC output [8].

To generate the inverter AC output, select harmonic cancellation to eliminate low order by optimizing the angle of the MLI [9].HHM-SAM exhibits lower THD for MLI converters at all resolutions [10]. MLI transformation using FPGA control has been proven to have the advantages of low design, high speed, strong adaptability and low hardware [11]. The FPGA-based control for the MLI provides similarity in the %THD of both simulation and experimental results [12]. In this study, VHDL codes were used in the design of 7-stage ladder inverter and H-bridge inverter circuits. The following sections describe the angle adjustment method and switch ladder multilevel inverter topology used to create the proposed 243-level AC output.

II. STUDY OF MULTI-LEVEL INVERTER TOPOLOGY

In this study, two topologies are considered to evaluate the 7-phase multilevel inverter. The topologies considered are hybrid bridge multilevel inverter and switch ladder multilevel inverter circuits. Both topologies use switches to control the level of the MLI circuit. Topologies are compared based on topology, number of switches used, and performance parameter. The following sections discuss MLI topologies.

i) H-Bridge Multi-Level Inverter

As the name suggests, MLI's H-bridge topology uses the "H" switching pattern, which is controlled by switching as required at Level 7 in the MLI. In each of the H-bridges, there are 4 switches to designate the voltage polarity. Based on the direction of the flow of current in the voltage source of the H-bridge, the 4 switches are ON and OFF to give the positive and negative voltage values for the levels. The voltage values for the H-bridge vary based on the level required in the MLI circuit. The Cascaded topology of the H-bridge provides an opportunity to series connect with another H-bridge to add up for higher levels of the MLI AC output. If the DC sources used in the H-bridges are of the same value, it is referred to as "Symmetrical"; and if the DC sources used in the H-bridges are of different values, it is referred to as "Asymmetrical". The DC value assignment can be based on the progression namely in powers of 2 to call it "Binary" or in the power of 3 to call it "Trinary". Depending on the value of the DC series used, the switching pattern of the levels will change. The schematic diagram of a 7-phase H-bridge cascade multilevel inverter is shown in Figure 1.

ii) Switched Ladder Multi-Level Inverter

Switched ladder multilevel inverter topology operates using the ladder pattern of switches. The switched ladder has two switches per DC voltage for its direction of operation. Based on the ON and OFF of the switch, the DC voltage value may be considered positive or negative. The number of levels in the output inverter should have more ladder circuits in the topology. The DC voltage values can be the same or in progression for the number of levels required. The switching patterns for the switch are the same for the switched ladder inverter as in the H-bridge Inverter. Figure 2 shows the topology of the switched ladder Multi-level inverter for 7-level.

In this study, a 7-phase multi-level inverter AC output field was designed using H-bridge and switching ladder topology. For the sake of controlling the inverter, the switch patterns are fed with the ON and OFF of switches. This is done using angle modulation as a non-carrier digital pulse width modulation. Traditionally, carrier-based pulse width modulation methods are used to design control switches. This work focuses on generating SAM-based switching designs using VHDL programming code and implementing them on FPGA devices. The designed switched synthesis VHDL code was analyzed using the synthesis method in the MATLAB Simulink tool.

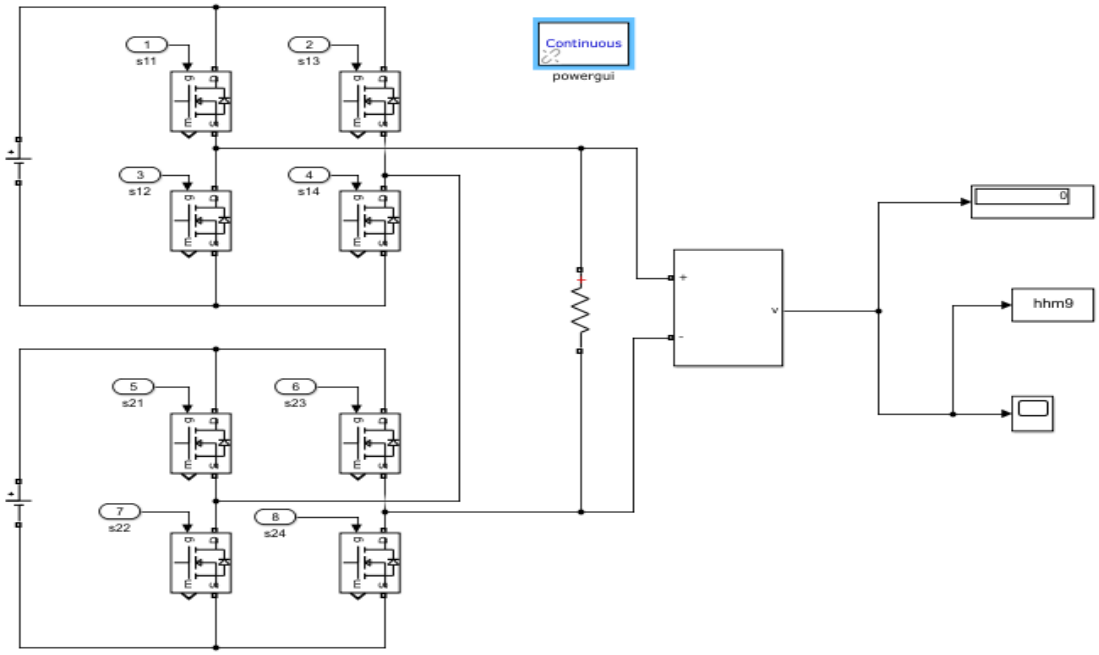

Fig.1 Circuit diagram for the 7-level H-bridge MLI topology

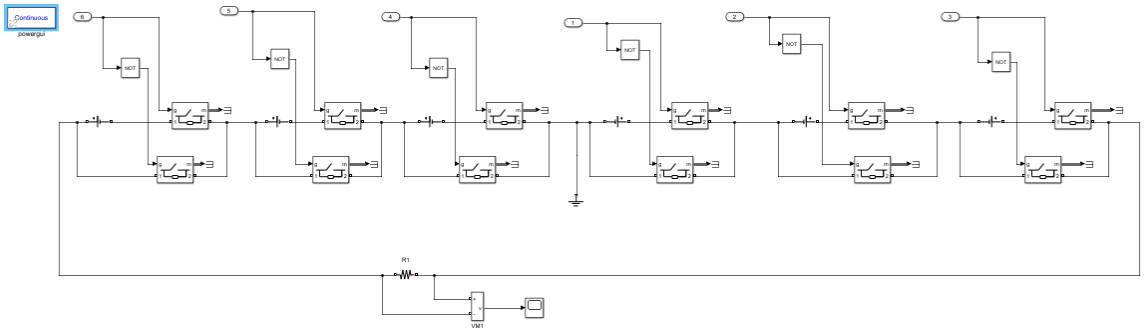

Fig 2 Circuit diagram for the 7-level Switched Ladder MLI topology

III. RESULTS AND DISCUSSION

The 7-level AC outputs are generated using the H-bridge and Switched Ladder topology using the non-carrier SAM algorithm. Among the SAM algorithms, the Half Height SAM algorithm is used for the switch pattern generations for its advantages for low THD% in the AC output of the MLI. The VHDL code for the HH-SAM algorithm is derived and equated digitally to

the resolution of 2^8 bits for developing the behavioural model of the code. Use a software generator to convert VHDL code that can be placed in Xilinx Simulink modules. Figure 3 shows the cross-compiled VHDL code of the MLI topology. The switching structure of the MLI circuit and the switches that will feed the MLI are shown in Figure 4. In 7-level Switch ladder topology, the number of switches used is only 6 (3 positive switches and 3 negative switches). The complementary switching of these 6 switch patterns is produced by the Inverter circuit in the topology. The number of switch patterns for the H-bridge is more compared to the switched ladder topology as given in Fig 7. The % THD is 12.52 and the same for the 7-level MLI circuit using the SLM and H-bridge is shown in Figure 5 and Figure 8 respectively. The parametric analysis for the presented methods is produced in Figure 6 for the SLM and in Figure 9 for the H-Bridge topology. The V_{PEAK} and V_{RMS} are meritorious for H-bridge over the SLM method as evaluated.

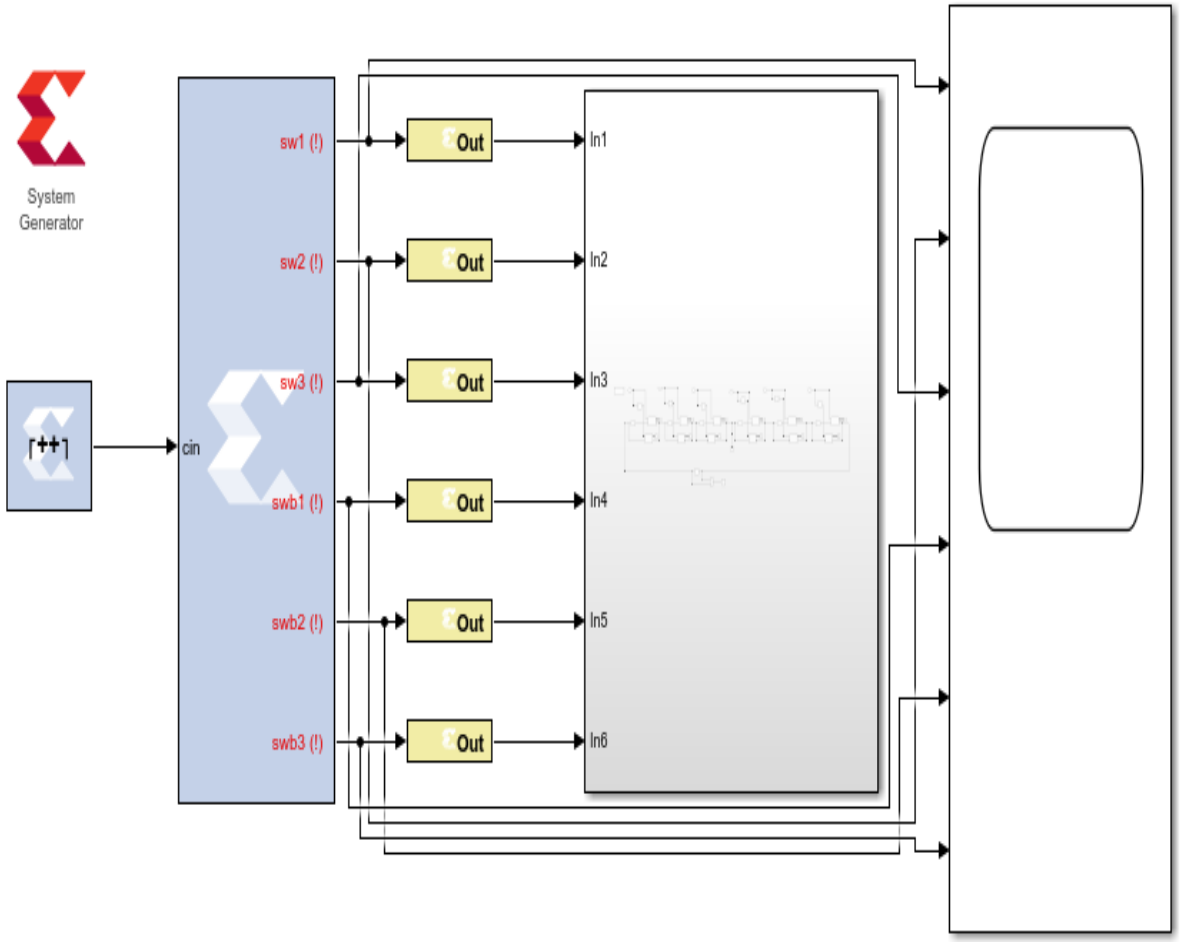

Fig. 3 MATLAB SIMULINK Model for the 7-level MLI using System Generator Tool

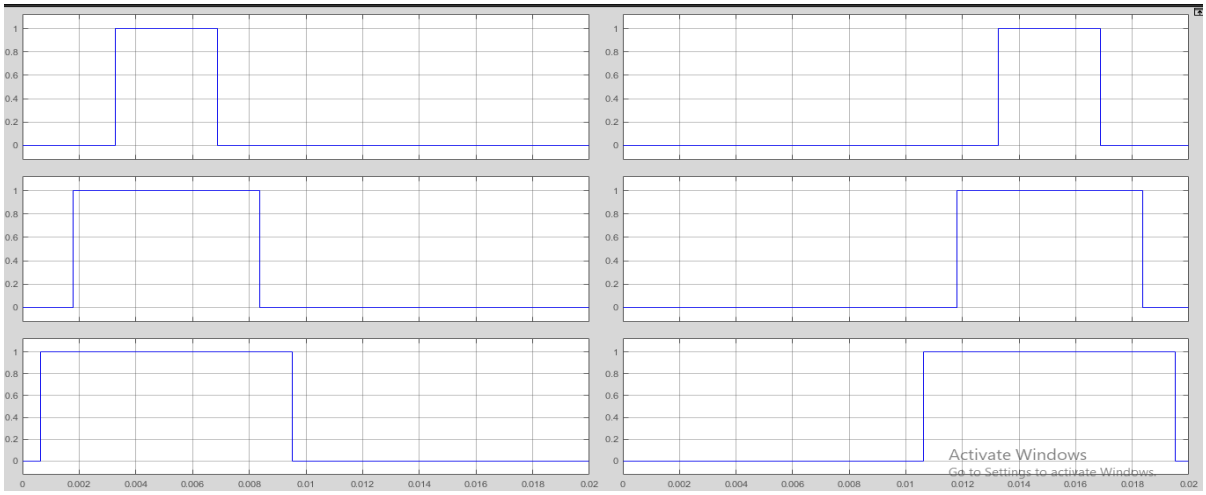

Fig.4 Switch patterns for the 7-level MLI AC output using SLM Topology

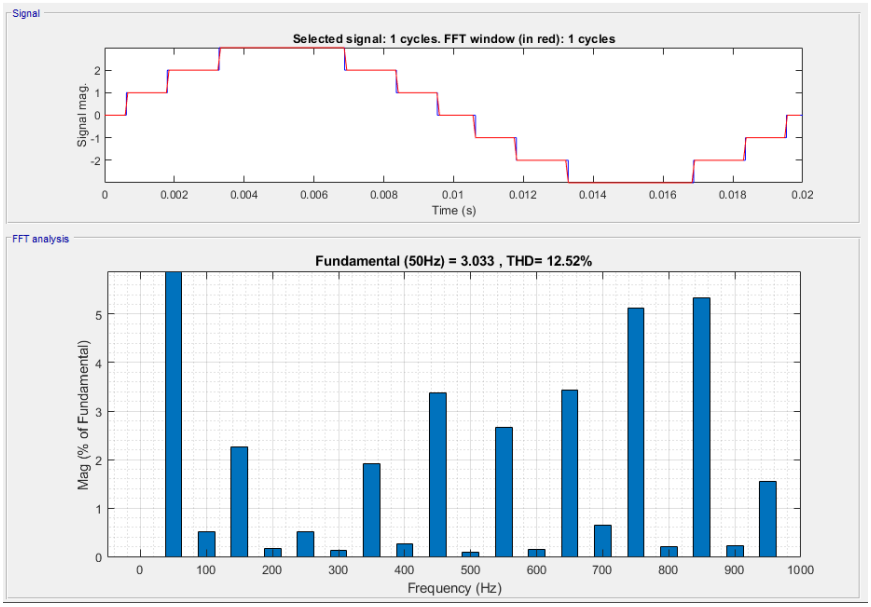

Fig. 5 %THD for the 7-level MLI AC output using the SLM Topology

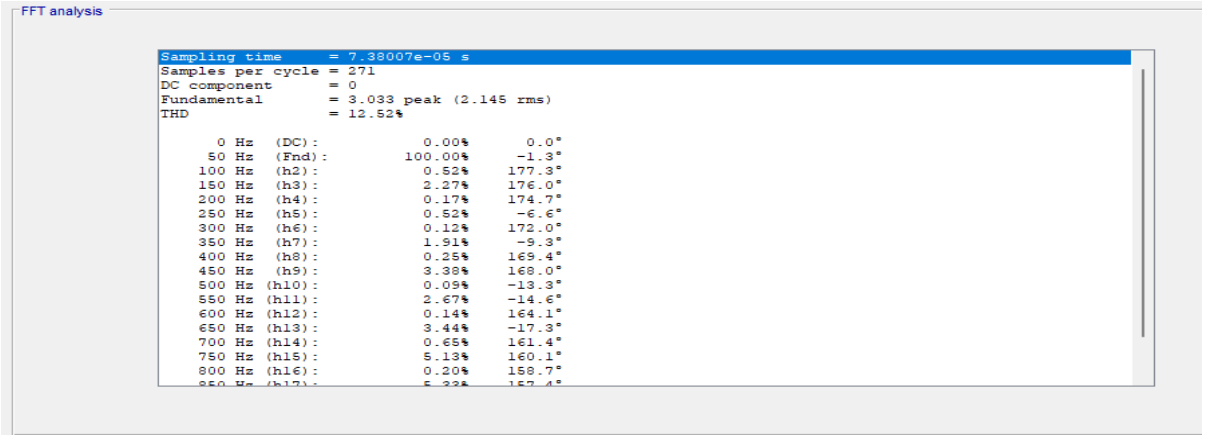

Fig. 6 Parametric evaluation for the 7-level MLI AC output using the SLM Topology

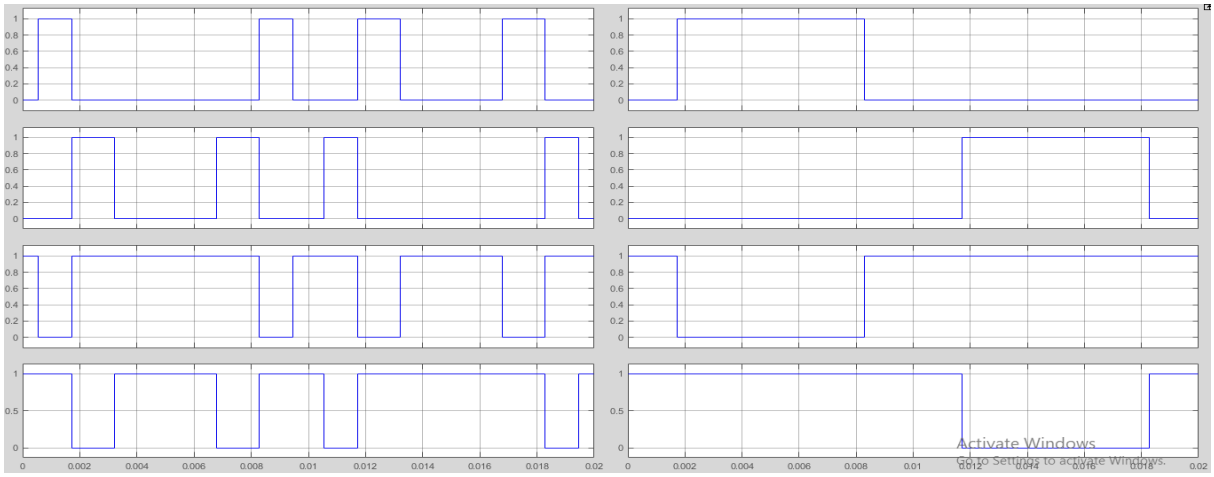

Fig 7 Switch patterns for the 7-level MLI AC output using H-bridge Topology

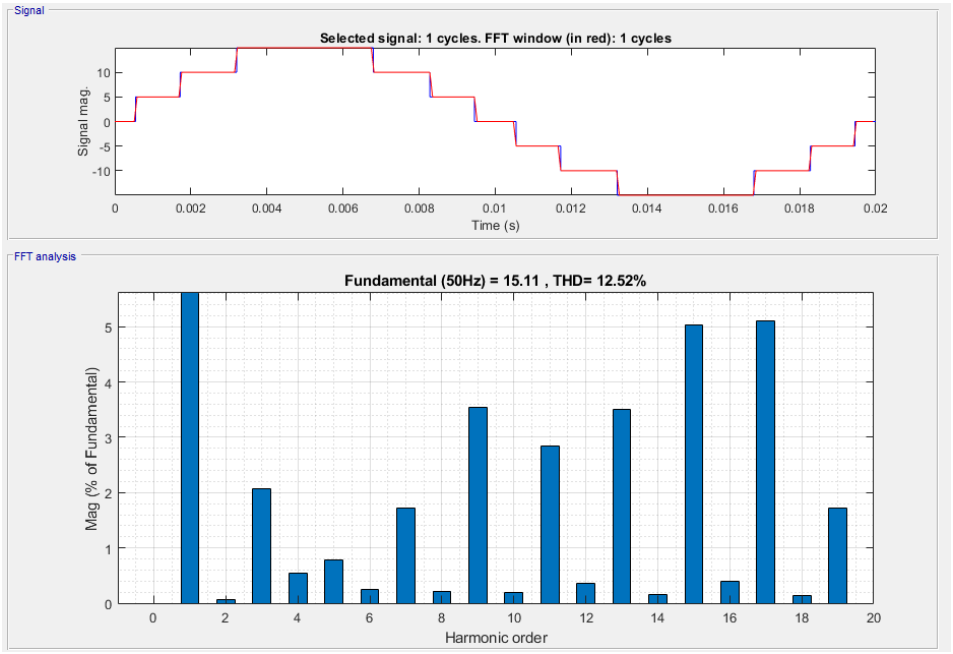

Fig 8 %THD for the 7-level MLI AC output using H-bridge Topology

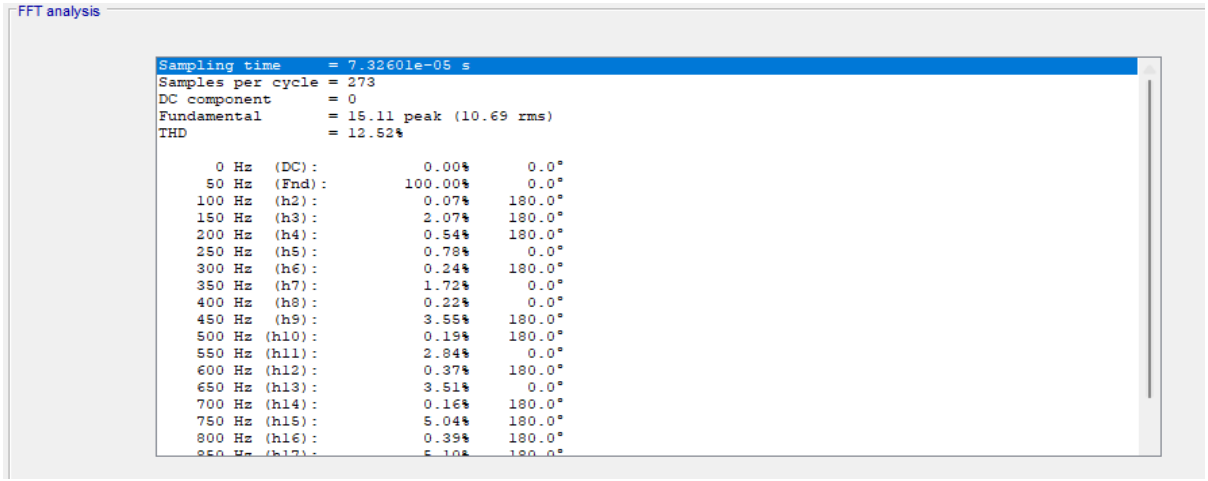

Fig. 9 Parametric evaluation for the 7-level MLI AC output using the H-bridge Topology

IV. CONCLUSION

This article compares 7-phase MLI AC output using switch ladder topology and H-bridge topology. For verification purposes, the cross-assembly of the synthesized VHDL code was imported into the Simulink module for simulation. The % THD for both topologies are the same at 12.52%, whereas the parameters such as VPEAK and VRMS holds good for the H-bridge topology, but the number of the switch is low in SLM. Overall these topologies can be used for the analysis of faults using Machine learning and Deep learning algorithms in real time.

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Author Biography

Nithya Ramalingam was born in 1989 in Cuddalore, Tamil Nadu. She obtained a B.E [Electronics and Communication] degree from Anna University in the year 2010 and an M.Tech [Embedded Systems] degree from Sathyabama University in the year 2012. She has put in 6 years of service in teaching. She is currently a Research Scholar in the Department of Electronics and Instrumentation Engineering at Annamalai University, Chidambaram, Tamil Nadu, India. Her research interest includes VLSI design, development of digital control for converters, FPGA implementation of control algorithms, and renewable energy sources-based power converters for real applications.

Anitha T received her B.E., M.E., and Ph.D. degrees in Electronics and Instrumentation Engineering from the Annamalai University, Chidambaram, India in 1998, 2005, and 2017 respectively. She is currently working as an Associate Professor at the Department of Electronics and Instrumentation Engineering, Annamalai University, India since 1999. Her current research interests include power electronic converters, renewable energy systems, process control, and embedded systems. She published more than thirty papers in international journals and also has more than ten years of research experience in the area of power electronics.

M. Arulaalan was born in Pondicherry, in 1980. He received a B.Tech degree in Electronics and Communication Engineering from Pondicherry Engineering College in 2001, an M.E. degree in communication systems from Thiagarajar College of Engineering in 2005, and a Ph.D. degree in Electronics and Communication Engineering from Pondicherry Engineering College in 2018. He is currently working as a Professor at the Department of Electronics & Communication Engineering, CK College of Engineering and Technology, Cuddalore. He has authored or co-authored over 20 publications (books & book chapters, journal articles, and conference papers). His research interests include Electromagnetic theory, Microwave devices and micro-strip antennas.

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