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Package Board Co-Simulation Using Equivalent Circuit Modeling Method for High-Speed System

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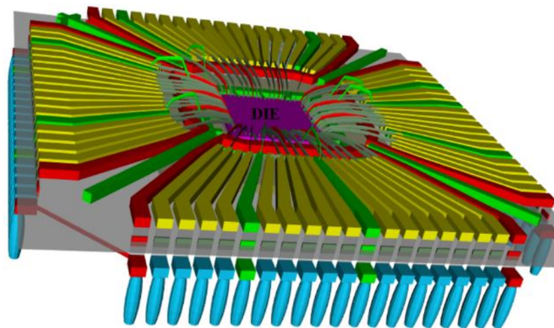
Abstracts: This research paper focuses on the challenges of system-level simulations for high-speed data transfer and the importance of modeling methodology in achieving accurate results. The simulating of PCB alone without considering the package model is not enough. Instead, to ensure optimal system performance, simulating the packages and PCBs together is essential. When simulating the high-speed parallel bus at the PCB level, it's crucial to consider the package model. If the package model is missing, achieving successful results can be challenging. In this paper, a method is proposed for developing a package model that is specific to the nets required for simulation purposes. The paper explores the challenge of simulating high-speed interfaces with a DDRx example that includes an RLC package model. An interconnect model technique is developed to apply the package RLC model through the equivalent circuit modeling method for the high-speed DDRx test board. This solution aims to simplify the co-design process by using simulation and verifying the model with the assistance of an eye diagram of the data bus. The proposed package model reduces jitter in co-simulation and ensures timing compliance for high-speed interfaces.

Keywords: High-Speed Interfaces, Printed Circuit Board, Double Data Rate, Co-Simulation.

1. INTRODUCTION

Electronic packages are used to connect semiconductor devices and printed circuit boards (PCB) by providing electrical paths for power and signal transmission. High-speed packages have become more complex, leading to increased complexity in devices and systems, multi-layered structures, and high-density I/O routing [1]. However, there are significant discontinuities between PCB and package interfaces, and PCBs can add extra return loss and bandwidth limitation, which can reduce system performance [2]. To ensure optimal system performance, it is essential to simulate both the packages and PCBs despite the challenges of complexity, discontinuity, and degradation [3]. Simply simulating the package and PCB separately and then combining them to estimate overall performance is not enough because this approach ignores the significant discontinuity between the package and PCB. A package serves as an interconnect structure that connects the IC dies to external circuits on the PCB while providing a protective structure for the IC dies. The package interconnect must be well-designed for successful signal propagation at the packaging level for high-performance transceiver channels [4]. A typical multilayer wire-bond packaging structure includes bumps, transmission lines, micro vias, and BGA balls, as shown in Figure 1, a cross-sectional view of the package.



Figuer:1 Lead Frame wire-bond package cross-section

When designing transmission lines, there are two types: microstrip and stripline, depending on the routing layer. Power and ground planes must meet power integrity requirements, including low loop inductance [5]. In multilayer BGA packages, vias and BGA ball pads have strong capacitive coupling with the ground planes of the entire package, especially at high frequencies [6]. Within the package, not all routed signals have equal lengths, resulting in different propagation times for each signal pin [7]. Therefore, the circuit board must take into account the delay of the package by adjusting the length of the signal carried at the circuit board level. The package device is often used as a memory device controller, and in such cases, the package pin delay is manually calculated and implemented in PCB routing. Before sending the artwork data to the manufacturer, the final stage of the board must be approved using a simulation tool once the routing is completed. However, the simulation tool has limitations in that it only understands the behavior model of the design in the form of an S parameter model for the package and PCB [8]. Providing the parameter and PCB models is crucial if the design relies on a packaged device. Performing simulations and completing the co-design flow PCB sign-off is impossible without this. To fill in the gap, the parametric model is used to simulate package delay. The simulation tool confirmed the suggested model and investigated the DDRx board, which operates at high speeds. This research paper also explores the challenge of simulating high-speed buses.

2. PROPOSED EQUIVALENT CIRCUIT MODEL OF MICROSTRIP STRUCTURE

When dealing with high-speed devices, it is crucial to remember that multiple signals and power/ground pins are involved. The connections between the die pins and the package pins are established through either microstrip or stripline technology, and each package pin has its unique RLC delay type of connectivity [9]. To ensure proper routing for high-speed DDRx interfaces on a PCB, it is essential to take into account the package delay values associated with each pin during the trace length compensation process. The length and delay values for the package pins can vary. Therefore, the trace length of the PCB must be modified accordingly during routing to compensate for these differences. Failure to do so can result in a mismatch of lengths of the high-speed nets on the PCB, leading to simulation failure and time violation reporting. To circumvent such issues, a package model must capture and specify the package interconnect delay for simulation tools [10].

In most cases, device suppliers provide a package delay report in the form of a datasheet file of each pin, which must be carefully considered and accounted for during the design process.

This paper's proposed 8-data lines model includes strobe and mask signals for better understanding. The interconnects of the package are connected to the central die of the package through the BGA ball. The package balls are connected to a leading die with interconnect lengths that are not matched. The test package contains over 472 solder ball pins. Figure 2 shows the equivalent circuit of unit length of the package interconnect line for developing the transceiver propagation delay model. The method suggested for the interconnect lines model includes all the necessary data required for any simulation tool. This includes detailed information about pin RLC models of interconnect lines and signal data obtained from the package pins.

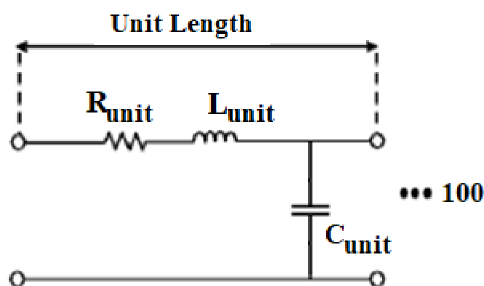


Figure 2: Equivalent circuit of unit length of the package interconnect line model

In order to accurately depict the interconnection line between microstrip line structures, a highly effective equivalent circuit model based on RLC components is utilized. In this model, the length of each unit is carefully designed to be less than λ/20, and a total of 100 precise units are incorporated to divide the length of the package interconnect. Each individual unit length is meticulously modeled using a series of advanced mathematical equations, ensuring a highly accurate and reliable representation of the interconnection line and mathematical equations.

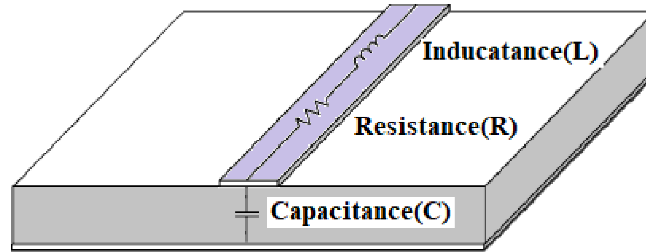


Figure 3: Package geometry

This paper creates a precise microstrip interconnection line structure model using an equivalent circuit model method consisting of RLC components. The primary focus is on accurately modeling the RLC in the microstrip line, which is a crucial factor in any interconnection line. The interconnection line and ground plane resistance were considered to achieve an accurate model. Figure 3 shows that most equation parameters can be easily measured on the package geometry.

$$R_{pack} = R_{(\text{ trace})} + R_{(\text{ ground })} \quad (1)$$

$$R_{(\text{ trace })} = \frac{L}{\sigma W T} \quad (2)$$

$$R_{(\text{ ground })} = \frac{L}{\sigma G} \quad (3)$$

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad (4)$$

However, realized that microstrip lines with different geometries require different equations for parasite calculations. For instance, Equation (1) is used to calculate the package interconnect resistance (R_{pack}), while Equation (2) and Equation (3) is used to calculate each component in Equation (1). Signals tend to transmit on a conductor's outer surface due to the skin effect at higher frequencies. Equation (4) is used to calculate the value of δ, which is a crucial parameter for our model.

$$\frac{L_{pack}}{\mu_0} = \left[-6.9 \times 10^{-5}\left(\frac{W}{H}\right)^{-4} + 0.4\left(\frac{T}{H}\right)^{-0.02} - 0.455\right] \times$$

$$\exp\left(-2.19\frac{S}{H}\right) + \left[1.04\left(\frac{W}{H}\right)^{-0.141} - 0.724\left(\frac{T}{H}\right)^{0.0086}\right] \quad (5)$$

$$\frac{C_{pack}}{\varepsilon_0} = \left[1.02\left(\frac{W}{H}\right)^{1.04} + 1.24\left(\frac{T}{H}\right)^{0.052}\right] +$$

$$\exp\left(-2.86\frac{S}{H}\right)\times\left[0.563\left(\frac{W}{H}\right)^{0.071}+1.96\left(\frac{T}{H}\right)^{1.23}\right] \quad (6)$$

Equations 5-6 accurately depict the inductance L and capacitance C within proposed model. Equation (5) was used for calculating L, while equation (6) was used for calculating C. After obtaining each component, it was segmented into unit lengths, as demonstrated in Figure 2. To determine the value of each component in a unit length, one must divide the total length of the line mentioned in the datasheet by the targeted number of units. Maintaining accuracy and attention to detail in these calculations is essential to ensure optimal results. In order to accurately model RLC, it is imperative that the unit length be less than λ/20. For this purpose, divide it into 100 units. This approach ensures that the model accurately represents the physical behavior of the system being analyzed. A packaging model of the test device is developed by utilizing these equations. This model should contain all the necessary information for the simulation tool to use during the simulation process. The proposed package model file contains information on package pin interconnect length and RLC. It closely resembles genuine package models and has been verified and compared.

3. EST BOARD AND TIMING PARAMETERS OF HIGH-SPEED BUS

A test board was developed, a highly advanced networking application system that boasts 32-bit DDRx DIMM. Each of the 32-bit DDRx interfaces is connected to multiple SDRAM devices, with each SDRAM device managing 16-bit data lines. During the design of this board, an 8-layer stack-up was utilized. The test board was expertly controlled by a controller device, and a visual representation of the system can be observed in Figure 4.

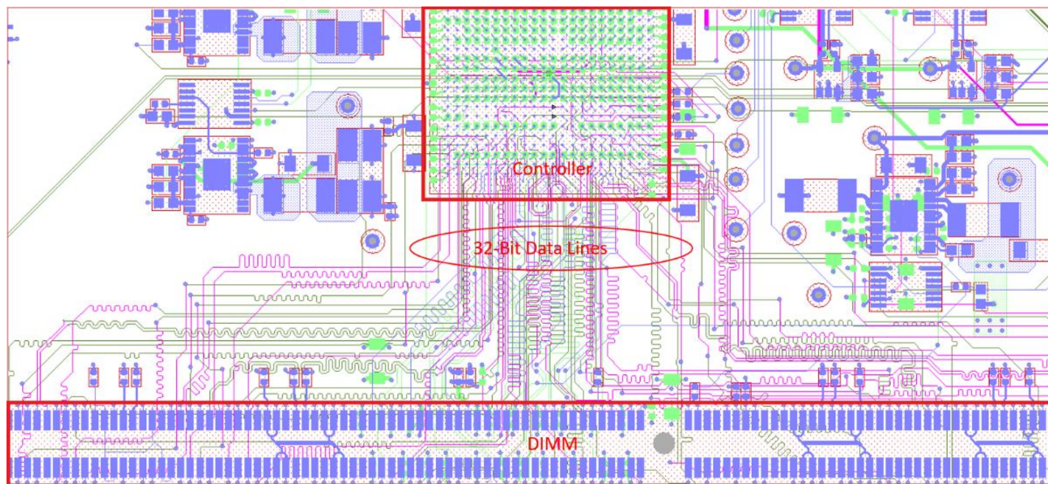


Figure 4 DDRx interface test board

The controller package exhibits non-uniform trace lengths for its pins, which may result in timing issues for high-frequency signals. To mitigate this, package de-skew is of utmost importance, particularly for the four length-matching data groups in the 32-bit DDRx interfaces. Each group comprises 8 data lines and differential strobe lines. Package delay must be accounted for in all traces to align the skew in each group. Each data line has a distinct interconnect delay, so the PCB board routing must adjust line length to compensate for package delays. All four data groups on the PCB must have their package delay compensated to match with a small tolerance value within a DQS group. Each pin delay in the package has been compensated for, resulting in a unique delay value on the data line of the PCB.

S parameters are important when simulating and verifying high-speed printed circuit boards. These PCBs contain numerous components and traces that require precise modeling, including microstrip, strip lines, and vias. High frequencies make measuring transmission and reflection parameters easier than voltage, current, and impedance. By utilizing S parameter settings, treat the system as a black box and measure its performance under various source and load conditions. This approach guarantees signal integrity on high-speed interfaces for PCBs,

and advanced simulation tools can be employed to measure performance in terms of gain, loss, and reflection coefficients. Furthermore, importing the S parameter file allows for further analysis, and cascading S parameters enables complete characterization of an interconnection path that includes package and PCB traces [12]. To extract S parameter models from the DDRx PCB, the Sigrity tool was used. Calculate the data bus's insertion, and reflection loss using these behavior models. Figure 5(a) shows the data group insertion loss, with a performance of .35dB up to a frequency of 1.6 GHz for all data line signals. The return loss of the data group remains around -15dB across the entire operational frequency range, as illustrated in Figure 5(b). Resonant peaks occur at 1GHz intervals due to routing constraints necessary for changing routing layers. The data lines s-parameter results contain the behavior model of the PCB interconnect, which is necessary for the simulation tool.

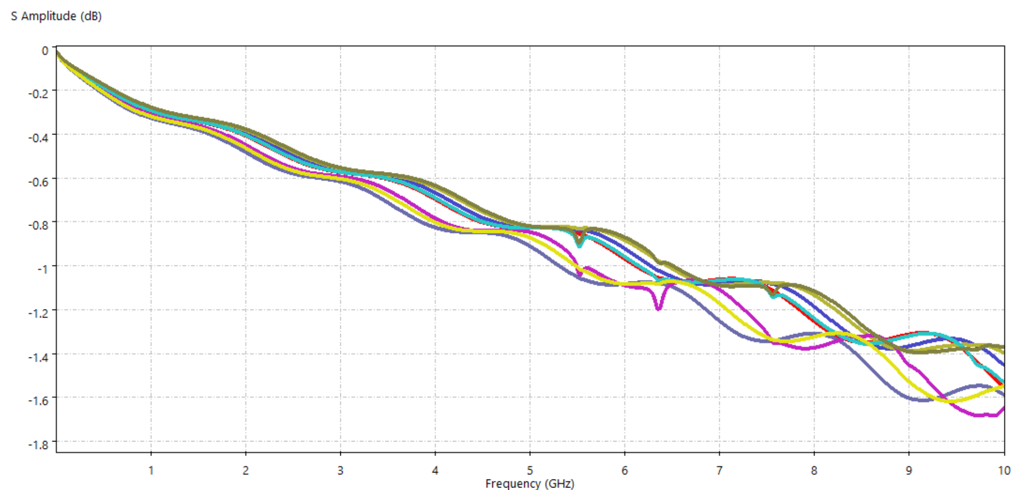


Figure 5(a) Insertion loss

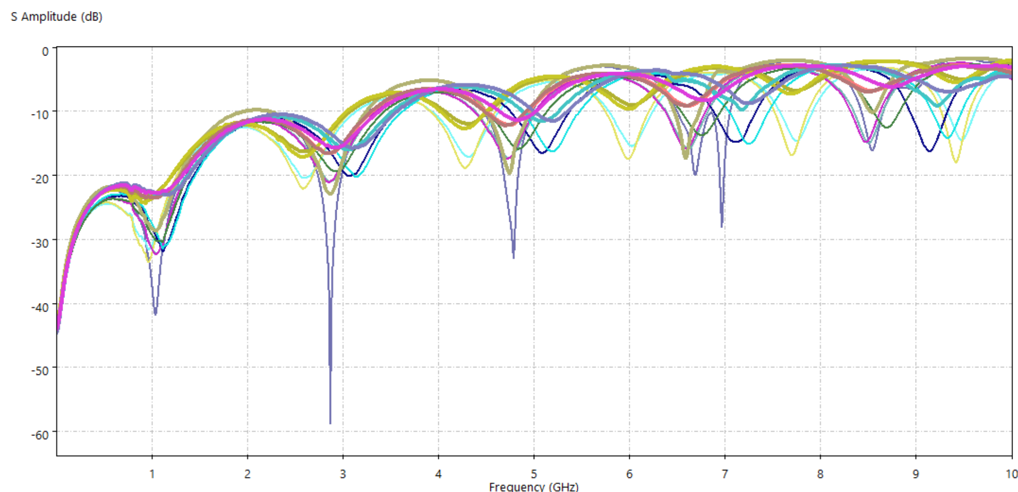


Figure 5(b) Return loss

To ensure the proper functioning of the high-speed parallel bus, it is crucial to have accurate timing. The best way to achieve this is through timing simulation. In a source-synchronous system, the clock and data signals come from one transmitter chip and travel through the package/PCB interconnect system [11]. They experience a delay before reaching the receiver chip. To ensure that the receiver chip accurately locks and samples the input data, the clock and data signal must be properly aligned, with a specific relative delay between them. Figure 6 explains the timing parameters for the DDRx bus. The Data UI, which represents the bit period of data signals, is calculated by taking the reciprocal of data rates. The transmitter uncertainties refer to the timing differences between the fastest and slowest output edges on data signals, which include data/clock output variation, clock skews, and jitters. These

uncertainties are known as TX_SETUP and TX_HOLD. The sum of all receiver requirements for a valid sampling window, during which the data must be valid to capture it correctly, is defined as RX_SETUP and RX_HOLD. Determining the strobe's position within the sampling window depends on the setup and hold times. Finally, the strobe signal determines the timing parameter for a bus to pass or fail. If it shifts the right or left side of the center point of the data eye, it means the timing parameter does not meet the parallel bus specification, resulting in data loss or timing violation.

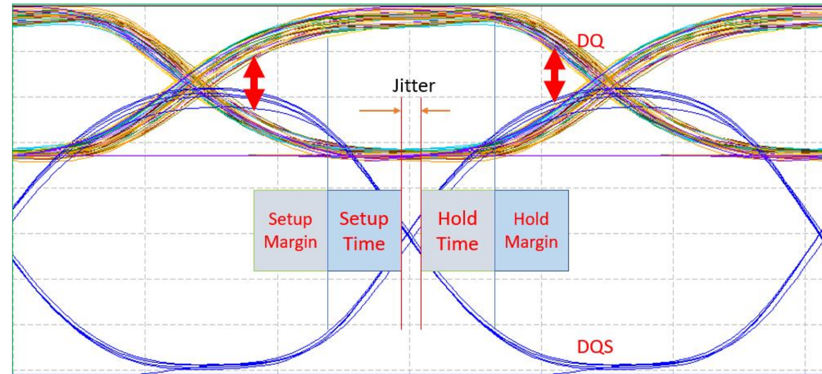


Figure 6: Timing parameter of high-speed parallel DDRx bus

To ensure accurate sampling of input data by the receiver memory chip, the sum of TX_SETUP, TX_HOLD, RX_SETUP, and RX_HOLD must not exceed the data UI. Having a positive setup and hold time margin during timing verification is also important.

4. VERIFICATION OF PACKAGE CIRCUIT MODEL AND RESULT DISCUSSION

The Sigrity tool was used to conduct two simulations in order to verify the package model. One simulation included the proposed package delay model, while the other did not. The results from these simulations were subsequently compared. The combined circuit model of the package and PCB are displayed in Figure 7. The package model is developed, and s-parameters are extracted from the test board. The package model includes the length and RLC component details as specified in the proposed model.

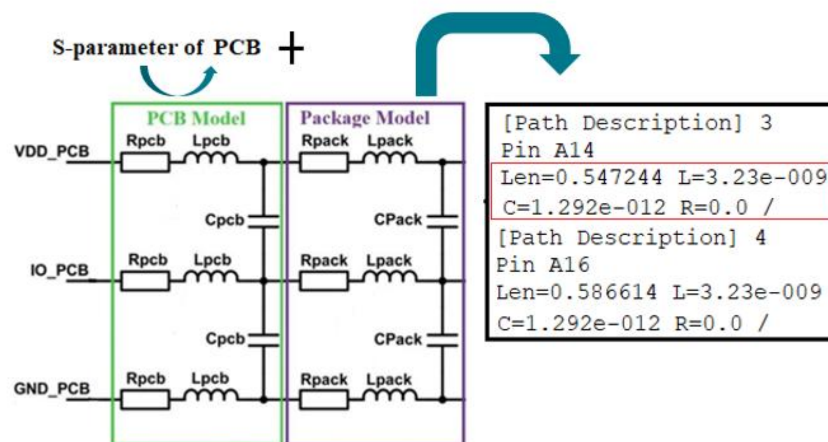


Figure 7 Equivalent circuit model for package and PCB.

S-parameters were extracted from the PCB and DIMM board for a data set. The extracted s-parameters were assigned to their respective blocks in the test bench, with the power-aware IBIS model assigned to the controller and memory device and the vrms block assigned to the control device and memory devices, as seen in Figure 8(a).

The test bench was set up with the appropriate setup and hold times for each device, and the simulation was run at 800MHz.

The transmit setup should have a timing budget of at least 0.25 seconds. On the other hand, the receiver setup and hold time should be budgeted at 0.16 ns. The skew budget was allotted 0.02ns for setup and 0.105ns for hold. The maximum receiver skew allowed during the reading process was 0.25 unit intervals (UI). The simulation utilized a 128-bit sampling rate pattern running at 1.6 Gbps, and the minimum number of bits required was 10101010. The package model, along with the test PCB s-parameter model, was run by the simulation tool and verified the eye diagram of data lines.

Figure 8(b) features the eye diagram where the reference strobe differential pair signals shifted, and the eye of the data group shrunk. Due to the mismatched signal length of this group on the PCB for an 8-data line group, the jitter of the data group is .035ns, as marked in Figure 8(b). Due to compensating for package pin delay on the PCB interconnection line by adjusting signal interconnection length, the data bus exceeded its .02ns timing budget. The setup and hold timing were violated by maximum data lines. The timing reference was shifted by 25.5ps from the simulated position to achieve the best-case timing, with a strobe adjustment resolution of 6.05ps.

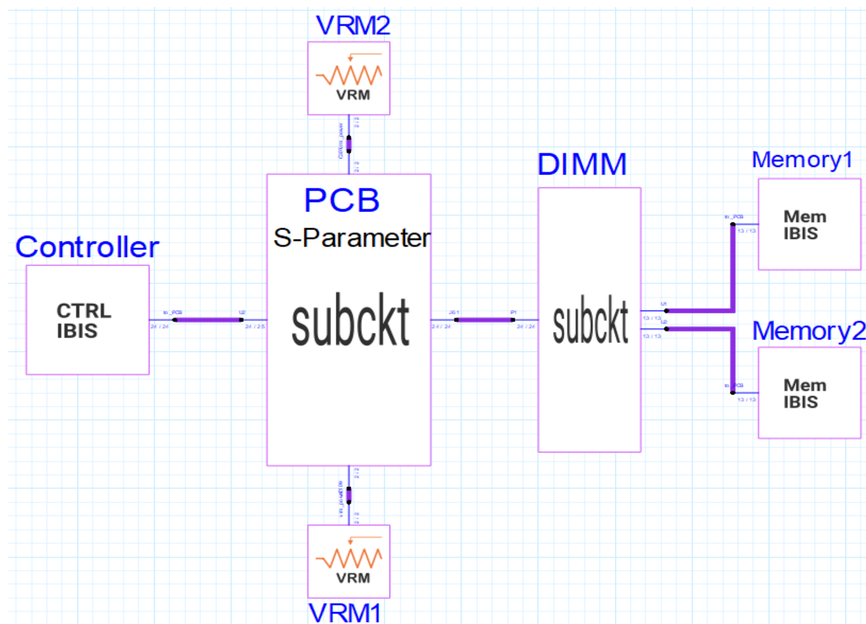


Figure 8(a) Simulation test bench setup without package model.

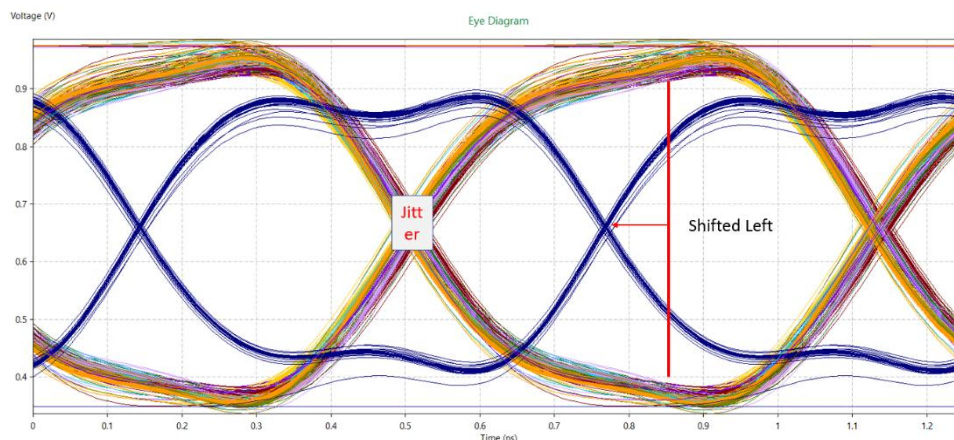


Figure 8(b) Simulation result of 8-bit data line with strobe signal

A second simulation was conducted by creating a parametric circuit model of the package to overcome this challenge. A new package circuit model block was inserted between the PCB and the controller block, storing the package interconnect delay information. The simulation was conducted at 800 MHz using the same settings as the previous simulation. Figure 9(a) shows the test bench set up with a package model inserted between the controller and PCB block. After making the necessary changes in the test bench, rerun the simulation.

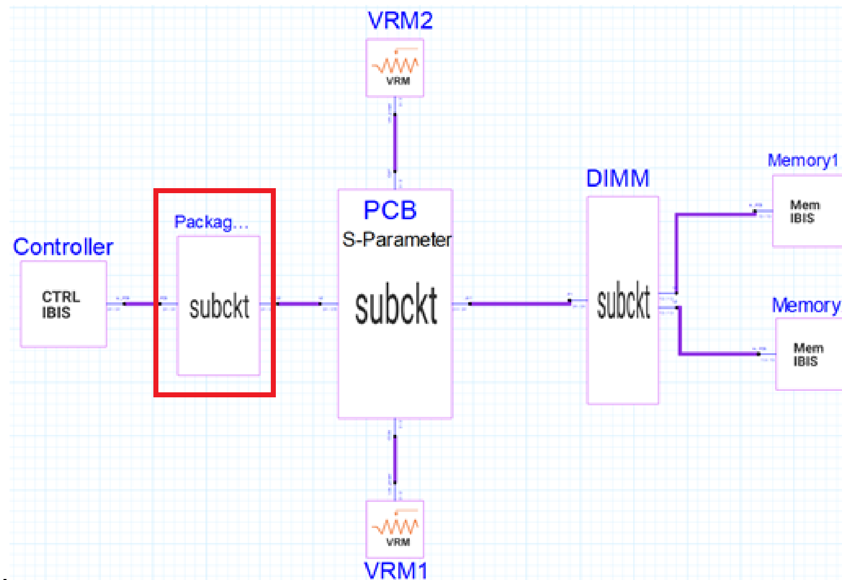


Figure 9(a) Simulation test bench setup for the proposed package model.

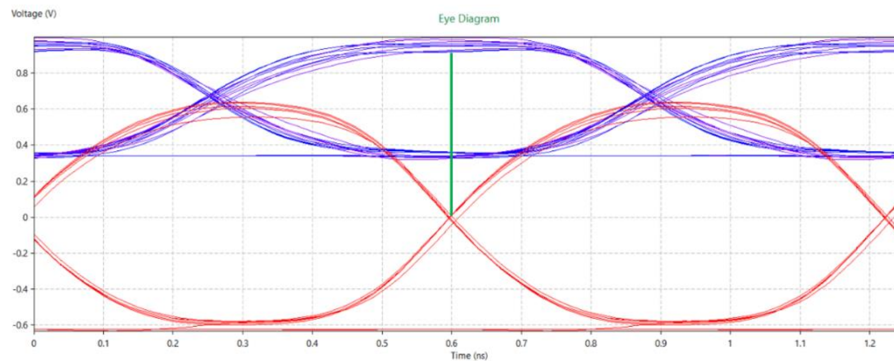


Figure 9(b) Simulated eye wave shape for proposed package model.

The eye diagram for 8-bit data lines is shown in Figure 9(b). The blue color represents the data lines, while the red color highlights the strobe signal. All 8-bit data signals are synchronized with the strobe signal, resulting in reduced jitter of .025ns, which is in the jitter budget range and improved eye-opening. The setup and hold timing are matched because the overall delay from the package to the PCB is taken into consideration. All 8 data lines met the timing parameters with respect to the strobe signals. During the simulation, the timing Ref was shifted by 105.38ps to obtain the best-case timing from the simulated position. Based on the simulation results, there are no signal timing violations, and all timing parameters have been successfully met despite signal failure during the preview simulation. The proposed package delay model accurately represents the interconnect delays, as confirmed by the simulation results. The simulation tool also considers the package model, which is demonstrated in the results.

CONCLUSION

The proposed method is a viable solution for developing a package model that can effectively simulate required nets, even when an IC model is unavailable. The equivalent circuit model has been thoroughly verified in the

frequency range of 100 kHz to 10 GHz, ensuring its reliability. The package RLC interconnect model has proven to be incredibly efficient in capturing interconnect delay, which has led to an improved jitter of the data eye diagram from 0.035ns to an impressive 0.025ns. The proposed solution for co-simulation of PCB and package systems is an excellent approach to studying the impact of PCB effects on system-level performance. It provides a strong foundation for future investigations if a package model is missing. Utilizing the proposed method effectively simulates high-speed data interfaces, leading to more accurate results and a better understanding of the system's performance as a whole.

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