Suppression of Simultaneous Switching Noise Using Embedded Capacitor Method in High-Speed Systems

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Abstracts: Gbps signals are commonly used in modern high-speed IO designs. These systems require a high level of signal accuracy. However, these signals can cause current fluctuations at high frequencies due to parasitic inductance on the package and board, leading to significant changes in supply voltage. DDRX interfaces that transmit data up to 4.8 Gbps induce simultaneous switching noise (SSN) in the voltage regulator module (VRM). One of the adverse effects of SSN is timing jitter, also known as power supply-induced jitter. The amount of SSN is directly proportional to the number of signals on a parallel bus. Discrete capacitors may not be effective in reducing SSN impact when data is transmitted at high speeds. The current approach used to predict and evaluate errors in SSNs relies on the designer's expertise, which requires accurate estimates of packaging parasitic. In this paper, a practical approach to lessen SSN is presented through the use of embedded capacitors placed between planes and optimizing discrete capacitors by connecting them in a way that measures the impact of supply noise on the I/O transistor circuit performance at the DDRX interface. Two boards were designed, evaluated, and subsequently compared their results.

Keywords: Simultaneous Switching Noise, Printed Circuit Board, And Power Distribution Network.

1. INTRODUCTION

The performance of high-speed systems is affected by switching noise caused by inductance in the power supply regulator. The performance of high-speed systems is influenced by switching noise generated by inductance in the power supply regulator. In a high-speed system, signals are switched at rates up to 4.8 Gbps, and discrete capacitors may be ineffective in reducing the noise at this rate. High-speed interconnect lines at the system level can be degraded by signal integrity issues, which negatively impact system performance. The PCB can be affected by external noise, but sometimes, the source of annoyance comes from within the IC. Even low-level ICs can experience noise in their output due to physical mechanisms. Parasitic elements in the PCB package can create unwanted noise in a circuit operating at high speeds and moderate levels. When an electronic device experiences simultaneous switching output noise, also called ground bounce, it may result in an undesired oscillation in the device's output, leading to an increase in errors in the received information, even if only one output is causing the ground bounce. Timing errors associated with setup/hold time violations are often linked to SSO and DDR interfaces.

High-speed digital circuits, like DDRX, experience high-frequency noise that affects signal quality and timing due to SSN increasing switching current, which impacts PDN. SSN is a significant concern in transistor-level circuits. Future designs with thousands of interconnects require complex modeling of SSN, which has already become a significant bottleneck in high-speed digital designs [1]. Parasitic inductance in the PDN of the high-speed interface, which often contains continuously switching signals at a very high data rate of up to 4.8 Gbps in package and multilayer printed circuit boards, causes SSN that adversely affects the performance of the interface [2]. At high data rates, the de-coupling capacitors, which are traditionally used to reduce or mitigate SSN, are ineffective [3]. Furthermore, quantifying SSN is typically complicated due to its heavy dependence on the physical geometry of the system [4].

The Equation describes SSN voltage. V_{SSN} is the simultaneous switching noise, N is the number of drivers switching, L_{eff} is the equivalent inductance in which current must pass, and I is the current per driver.

$$V_{ssn=}NL_{eff}\frac{dI}{dt} \quad (1)$$

The power supply must deliver enough current to satisfy the sudden demand when a large number of signals switch at the same time. The current passes through an inductance, L_{eff}, and introduces a noise of V_{SSN} into the power supply. SSN occurs at both the chip level and the board level. At the chip level, the power supply is not perfect [5]. The board-level power must supply any sudden demand for current through the inductive chip package and lead frame. On the board level, sudden current demands must be supplied through inductive connectors. Significant simultaneous switching noise (SSN) coupling occurs through the signal via transition when the signal vias suffer return current interruptions caused by reference plane exchange [6]. The coupled SSN decreases the noise and timing margins of digital and analog circuits, reducing achievable jitter performance, bit error ratio (BER), and system reliability. As a result, timing violation occurs due to core or I/O voltage fluctuation [7]. The plane coupling method introduced in this paper creates a high-value capacitance between the planes to minimize simultaneous switching noise coupling effectively. This method reduces the inductance path of the PDN. When switching activities happen, and current is drawn from voltage sources, the high-value capacitance between the planes stores and supplies charge to transistors.

2. SSN COUPLING MECHANISM THROUGH VIA AND TRACES

In a multi-layer board, a ground plane and a power plane can be used as the reference for signal trace. For example, interconnects of data lines in DDRX with multi-bit in-memory modules can take the different layers on the module. Figure 1 shows the simultaneous switching noise coupling mechanism through the reference changing vias in a typical 6-layer standard board. Reference changing vias must be used to transit between power or ground planes that require multiple layers for effective routing of many signals in a limited space. The reference changing vias, however, become the structures causing the simultaneous switching noise coupling to signal [8]. When driver chips consume a number of instant currents, the simultaneous switching noise generated near the reference changing via has a relation with power/ground cavity impedance near the via, which is frequency dependent. The higher the power/ground cavity impedance, Z, the higher the simultaneous switching noise voltage, V_{ssn}.

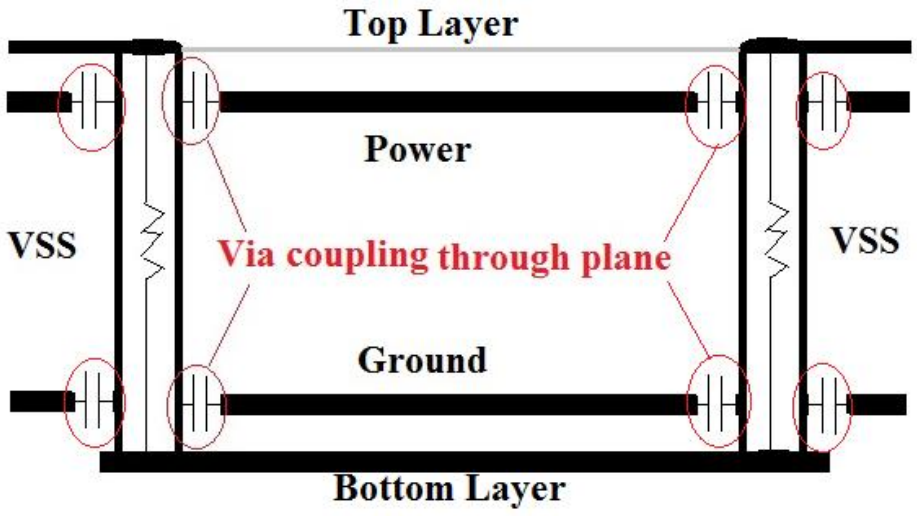

Figure 1: SSN coupling to signal by the signal via exchange reference.

The via coupling model is shown in Figure 2 for the 6-layer stack-up board. The electrical model of the metallic via column is expressed as an inductor. At the same time, the capacitive coupling between the via and the adjacent reference planes is modeled by coupling capacitors surrounding the metallic via column [9]. The signal vias are coupled equally to the power plane (layer 5) and the plane pair's ground plane (layer 2) in a balanced manner. The via-neck effect is added to the model by adding an inductor. This effect is induced by the absence of the reference plane under the signal trace at the via clearance [10].

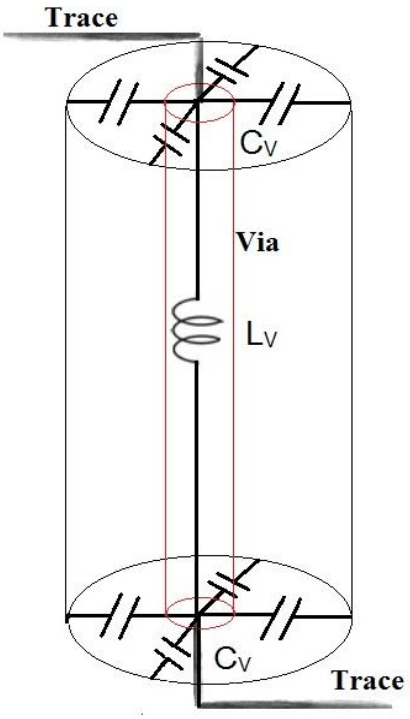

Figure 2 Via coupling model

When simultaneous switching noise is generated near the reference change via a plane pair, the time-varying simultaneous switching noise voltage is built up between the power plane and the ground plane [11]. Thus, simultaneous switching noise is developed across the two planes at the via position.

When a high-speed signal is routed between the noisy planes, the plane noise is easily coupled with the signal nets, as shown in Figure 3. A noise voltage is induced into the signal trace due to SSN coupling; line equation: 2 of the signal trace with impressed voltage and current has been derived as an equation: 3

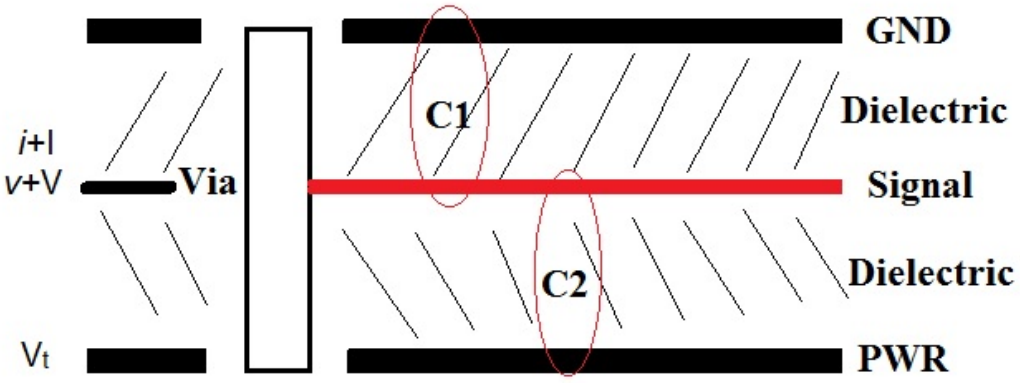

Figure 3 Transmission line between a noisy plane pair

$$-\frac{\partial i}{\partial x} = C_1 \frac{\partial (V+v)}{\partial t} - C_2 \frac{\partial v}{\partial t} - C_2 \frac{\partial (V+v)}{\partial t} \quad (2)$$

$$-\frac{\partial v}{\partial x} = L \frac{\partial (i+I)}{\partial t} \quad (3)$$

v represents the voltage, and i represent the current produced by the wave propagating along the signal trace. V_{ssn} represents the SSN voltage between the power plane layers, and V, I represent the voltage and current impressed on the signal trace by SSN. Capacitor C_1 is created between the signal and ground layer, and capacitor C_2 is created between the signal and power layer. Capacitors C_1 and C_2 are inversely proportional to the distance between the signal and plane layers. Coupling SSN noise depends upon the parameters of the signal trace, that is, L, C_1, and C_2.

On the other hand, the noise coupling impedance can be used for the time domain analysis. If a periodical switching current source I(t) is given in the time domain, its frequency spectrum I(f) can be calculated by Fourier transform [12]. The frequency spectrum of coupled noise voltage is a product of I(f) and the coupling impedance Z_{couple}. The noise voltage is superimposed on the signal voltage, which results in jitter and even logic faults in data lines [9].

$$V_{couple}(f) = I(f) \times Z_{couple} \quad (4)$$

To understand the cause of simultaneous switching noise, it's crucial to analyze the structure of a CMOS buffer, its connections with other CMOS buffers in the same package, and the interconnection of multiple ICs. Figure 4 illustrates the standard layout of a CMOS IC with buffer circuits. All of these CMOS buffers are linked to the identical GND net. The system's primary clock, which could be labeled as active, drives the various buffers and causes them to switch states, when several buffers are connected to the same GND net, a powerful oscillation is produced, disrupting the intended signal level.

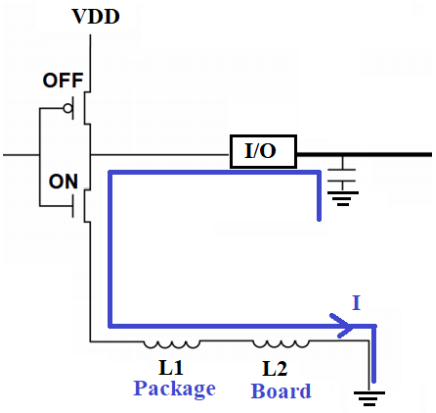

Figure 4 CMOS IC with buffer circuits

When multiple buffers are switched simultaneously, their noise can impact other circuits and lead to an oscillation that can be detected when measuring the output signal on the I/O line in relation to the GND net. The diagram below illustrates the current's path back to the ground during an OFF-to-ON switching event. Both the voltage loop and current path flows through a series LC circuit. If an inductor and capacitor in a circuit are arranged in series with low resistance, the transient response is likely to show an underdamped oscillation. This is a common occurrence in a series LC circuit with low damping. When it comes to high-speed digital ICs, multiple buffer switching can produce ringing behavior due to parasitic elements. One effective solution is to incorporate a bypass capacitor between the power and ground pins of the IC. The capacitor can discharge any excess charge and rectify the imbalance in the ground reference level.

3. METHODOLOGY

The present study analyzed two test structures, a 6-layered reference board, and a proposed board, as shown in Figure 5. Both boards use the DDRX interface. In the DDRX interface, all 32 high-speed data lines transmit data at the rate of 4.8 Gbps. There are two channels on the DDRX interface board. Each of those channels has a width of

40 bits: 32 bits of data with eight bits of ECC. While the data width is the same, having two smaller independent channels improves memory access efficiency. To use the DDRX model, simply plug it into the DDRX DIMM socket. Two voltage regulator components power the processor and DIMM module. During high-speed routing, all data lines are matched with the strobe signal to achieve the set and hold timing margin during read and write cycles of data on memory devices. In order to stabilize the core voltage of a processor, different values of de-coupling capacitors are utilized.

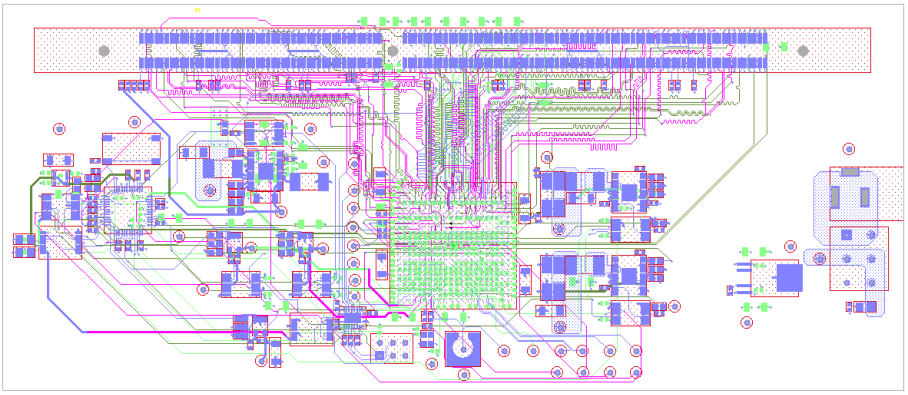

Figure:5 Proposed board layout

Figure 6(a) shows that the 6-layer reference board has a board thickness of 1.5 mm. The reference board has two pairs of plane layers. The dielectric thickness between these two plane layers is 35 mils, creating minimum inter-plane capacitance. When the data signal of DDRX memory switched with signals speed up to 4.8Gbps, the signal vias coupled with plane layers and injected SSN into VRM. Figure 6(b) shows the proposed 6-layer board has multiple sets of plane layers that are tightly coupled with another plane layer. The dielectric thickness between the plane layer further reduces to 5 mil, which creates high-value inter-plane capacitance. The proposed solution utilizes an integrated power plane capacitor method to minimize the effect of simultaneous switching noise. This integrated high capacitance at the board level effectively reduces the SSN effect.

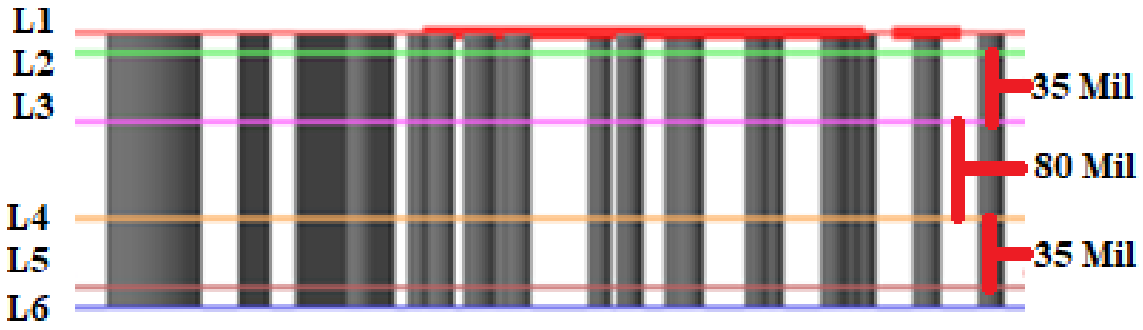

Figure 6(a): 1.5mm thick, 6-layer reference board.

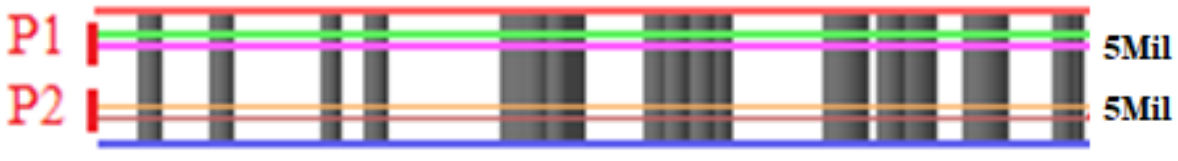

Figure 6(b): 1mm thick 6-layer proposed structure board

Figure 7 shows the result of the reference board when high-speed data lines in the DDRX channel are SSN injection switching simulations in the PDN. Channel 2 represents high-speed data lines, whereas channel 4

represents SSN noise introduced at the PDN voltage, VDD. The peak-to-peak noise voltage is 230mV during the data lines transition. Because the SSN noise induced at the board affects the signal integrity of the DDR interconnects and other high-speed interfaces on the same board.

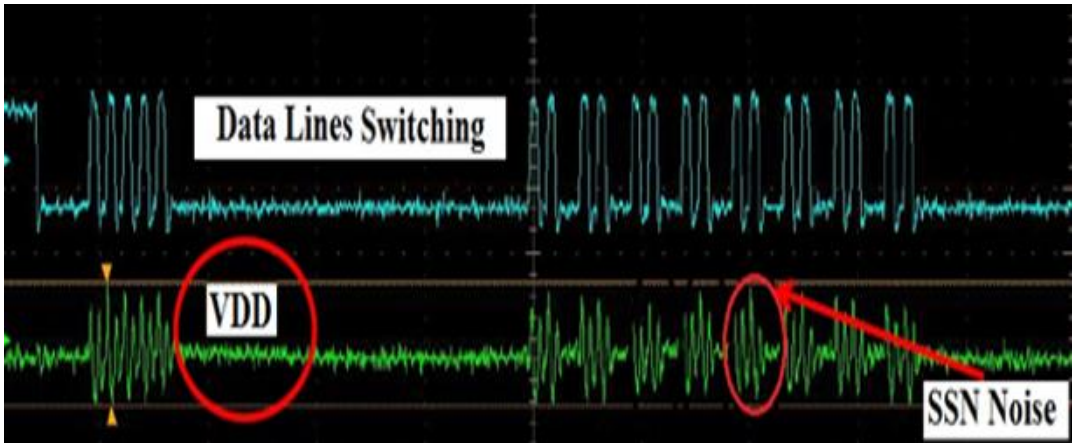

Figure 7: SSN induced in PDN when data lines switch simultaneously.

4. RESULTS AND DISCUSSION

The simulation tool extracts S parameters of 32 high-speed data lines with speeds of up to 4.8 Gbps from the two boards. Figure 8 shows the test bench setup in the system SI tool. The power-aware model is assigned to the controller and memory blocks. The S parameters of the DIMM board are also retrieved from the DIMM board. Two 16-bit memory is used in the test bench setup. The PCB S-parameter connected with DIMM models through a connected line. Two VRMs are used in the test bench setup in simulation tool, one VRM for the controller and the other for memory.

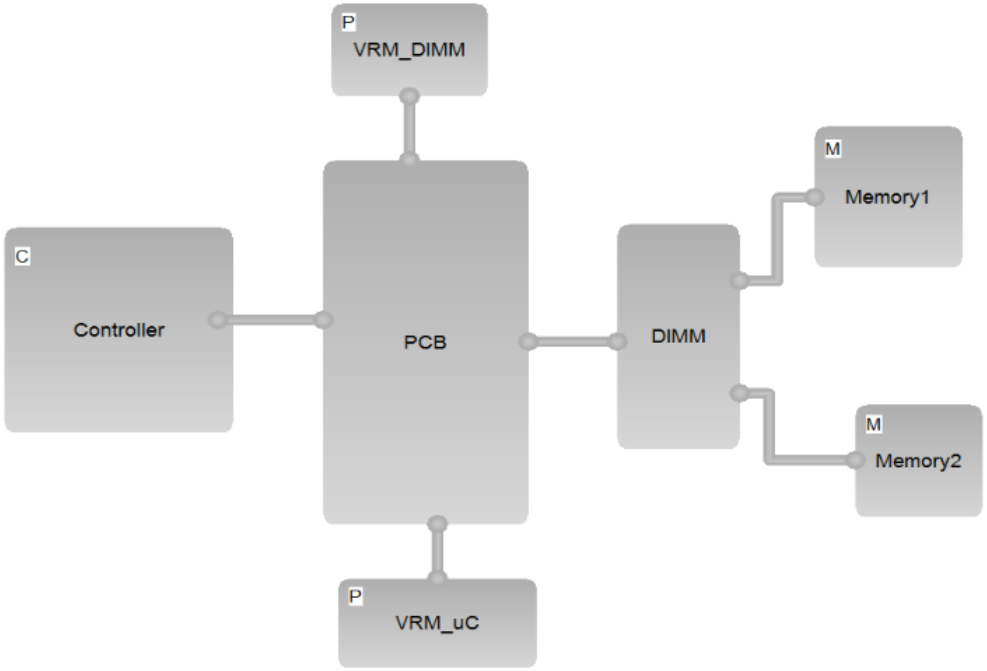

Figure 8: Test bench setup for DDRX simulation.

Due to the simultaneous switching of high-speed signals from the DDRX lines, the ripple effect of both boards played a critical role in the signal quality. The power ripple for the proposed structure and reference board was simulated using Sigrity tool. Figure 9 shows the power ripple for the reference board, and Figure 10 shows the power ripple for the proposed structure board. Figure 9 shows, the peak-to-peak voltage noise is 220 mV, which is 16% of the 1.35 V nominal voltage rail.

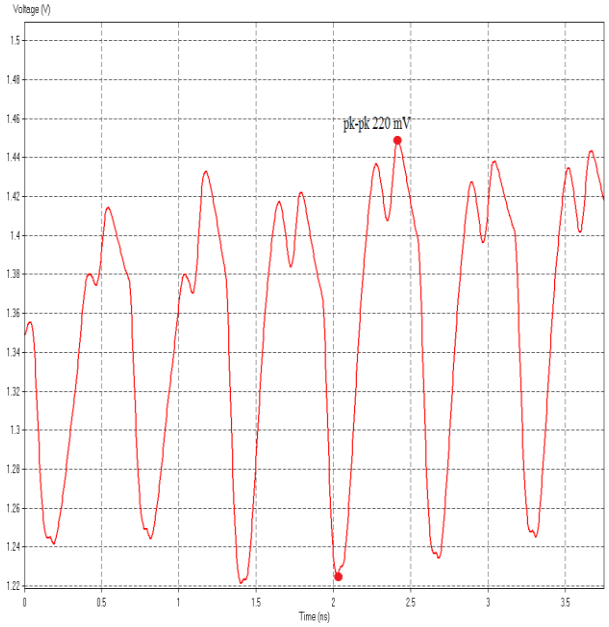

Figure 9 Power ripple plot for the 6-layer reference board.

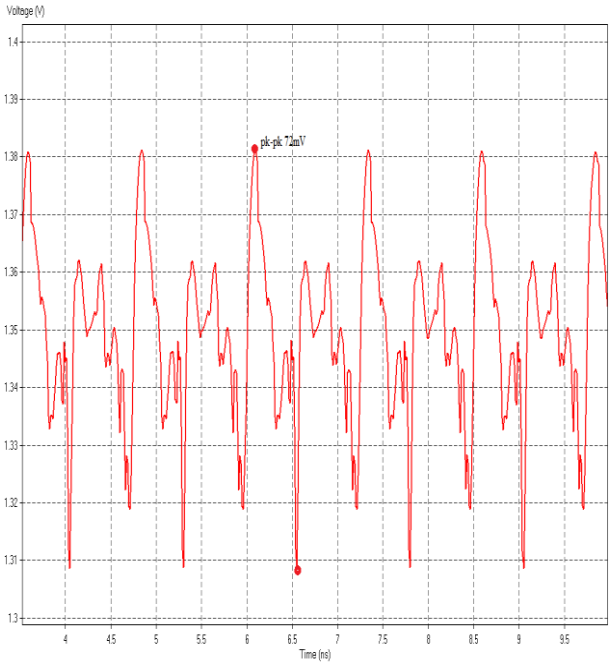

Figure 10 Power ripples plot for proposed structure board.

Figure 10 shows that the 72mV peak-to-peak voltage reduces when the integrated decoupling capacitor is introduced between the power and ground planes. The proposed method decreases dielectric thickness between the two power plane layers, thereby increasing the integrated capacitance between the plane layers and, as a result, is very effective for resonance frequency. By using thin layers, the proposed board results in a one-third

reduction of ripples in PDN voltage. Using the inter-plane coupling technique at the board's design level, the proposed method effectively reduced the SSN caused by the high-speed data bytes of the DDRX interface. In addition to the improved power distribution, the integrated capacitors of this method provide noise immunity.

CONCLUSION

The SSN effect must be comprehended and correctly accounted for in future high-speed designs. SSN effect introduces undesirable ripples in PDN, which can lead to the failure of high-speed systems if not resolved. The solution suggested in this research provides a practical and systematic method for identifying and implementing plane coupling for accurate analysis of the 4.8 Gbps interconnects in the DDRX interface. Simulation findings show that the strategies improve the power ripple parameter of the PDN by 150mV. Plane coupling capacitors are not only cost-efficient since they are integrated into the dielectric substrate but additionally have a high capacitance and are highly good at reducing the simultaneous switching noise effect. The proposed method successfully reduces SSN in DDRX high-speed interfaces.

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